IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Johannes P. M. VanLammeren	CONFIRMATION NO.:	5975
		DOCKET NO.:	NL020143US
SERIAL NO.:	10/505,350	EXAMINER:	Thomas J. Hiltunen
FILED:	August 19, 2004	ART UNIT:	2816
FOR:	INTEGRATED CIRCUIT		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL REJECTON

Dear Sir:

In response to the Final Office Action dated August 4, 2008, please amend the application as follows:

IN THE CLAIMS:

1-3. (Canceled).

4. (Currently Amended) A method of processing digital input data to produce digital output data using a processing circuit comprising flip flops, each flip flop comprising a first latch and a second latch coupled in series, the method comprising:

providing first and second non-overlapping clock signals;

computing said digital output data, comprising:

clocking first latches of said flip flops using said first non-overlapping clock signal; and

clocking second latches of said flip flops using said second non-overlapping clock signal; and

outputting said digital output data;

wherein the first latch and second latch of each particular flip flop receives said first non-overlapping clock signal and said second non-overlapping signal, respectively.

5. (Previously presented) The method of claim 4, further comprising:

producing multiple successively-delayed versions of the first clock signal;

producing multiple successively-delayed versions of the second clock signal;

clocking different subsets of the first latches using different respective ones of the successively delayed versions of the first clock signal; and

clocking different subsets of the second latches using different respective ones of the successively-delayed versions of the second clock signal.

6. (Currently Amended) Circuitry for processing digital data input data to produce different digital output data, comprising:

first and second non-overlapping clock signals;

means for computing said digital output data, comprising flip flops each comprising:

a first latch of said flip flops, said first latch being clocked using said first non-overlapping clock signal;

a second latch of said flip flops, said second latch being clocked using said second non-overlapping clock signal, wherein said first latches and said second latches are coupled in series; and

wherein the first latch and second latch of each particular flip flop receives said first non-overlapping clock signal and said second non-overlapping signal, respectively.

7. (Currently Amended) The circuitry of claim [[4]]6, further comprising:

means for producing multiple successively delayed version of the first clock signal;

means for producing multiple successively delayed version of the second clock signal;

a clock network wherein:

different subsets of the first latches are clocked using different respective ones of the successively-delayed versions of the first clock signal; and

different subsets of the second latches are clocked using different respective ones of the successively-delayed version of the second clock signal.

REMARKS

Entry of this amendment, reconsideration of all grounds of rejection in the Office and allowance of the pending claims are respectfully requested. Claim 4-7, as amended, herein, remain pending herein.

Applicant notes with appreciation the renumbering of claims performed by the Examiner. Claim 7 was amended to dependency was changed to depend from claim six, instead of claim four, in view of the renumbering of claims performed by the Examiner.

Claims 4-7 stand finally rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Sheen (U.S. 6,727,060). Applicant respectfully traverses these grounds of rejection for the reason indicated herein below.

Claims 4 and 6 have been amended to recite in part:

> wherein the first latch and second latch of each particular flip flop receives said first non-overlapping clock signal and said second non-overlapping signal, respectively.

Support for the above amendments is found at least at page 4, lines 5-11. By providing the first latch of each flip flop with a first non-overlapping signal and the second latch of each flip flop with a second non-overlapping signal. Some advantages of the claimed invention include reduced bounced, and no clock skew.

Applicant respectfully submits that Sheen fails to anticipate any of the present claims as it fails to disclose all of the claimed elements. Nor would any of the present claims have been obvious at the time of invention in view of Sheen.

For example, in each row in Sheen, the entire respective row receives a same "CX" clock sub-signal, but does not receive a second sub-signal. For example, referring

to FIG. 3 of Sheen, only sub-signal C8 is provided to the row 306A. Sub signal C1 is only provided to the same row 306H.

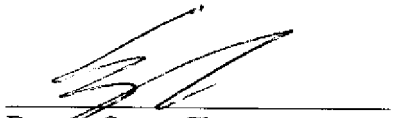
In contrast, in the presently claimed invention, in a same row, two respective non-overlapping clock signals are provided to each particular row.

Accordingly, Sheen fails to anticipate the presently claimed invention as the reference fails to disclose all the recited elements of the present claims.

For all the foregoing reasons, it is respectfully submitted that none of the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

Aaron Waxler
Registration No. 48,027



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By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Mail all correspondence to:
Aaron Waxler, Registration No. 48,027
NXP, B.V.
NXP Intellectual Property Department
M/S41-SJ
1109 McKay Drive
San Jose, CA 95131
Phone: (408) 434-3000
Fax: (408) 474-9081